

UNIVERSITY OF BOLTON
FACULTY OF ADVANCED ENGINEERING AND
SCIENCES
RAK CAMPUS
BENG(HONS) ELECTRONIC & COMPUTER
ENGINEERING
SEMESTER 1 EXAMINATION 2011/2012
COMPUTER ENGINEERING
MODULE NO: ECE3046

Date: Monday, 16 January 2012

Time: 2.00 – 4.00 p.m.

INSTRUCTIONS TO CANDIDATES:

There are 6 questions on this paper

Answer 4 questions.

All questions carry equal marks.

Marks for parts of questions are shown in brackets.

Unless otherwise stated all symbols take their usual meaning.

Electronic calculators may be used provided that data and program storage memory is cleared prior to the examination.

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1.

- a) Explain Cache Memory in terms of its significance to modern computing systems. (5 marks)
- b) A direct mapped L2 cache in a 32 bit system uses 1024 entries to hold 64 bytes of data. With the aid of a diagram show the virtual address format required identifying the position and number of bits in each field. (6 marks)
- c) During the execution of a program the above mentioned system accessed the main memory located by following 32-bit address:

181F2CE9 24F49B18 522E1E2C

During the subsequent execution the following addresses are accessed:

24F49B21 522E1E2C 181F2C21 24F49C21 181F2CF1 522E1D2C

Determine how many cache hits occurred. (14 marks)

Total 25 marks

2 .

- a) A 32-bit computer is installed with 16 MB of physical memory. A virtual memory operating system is also installed with the system. Assume the system uses 4 K page size. Explain with the aid of a suitable diagram how the MMU of this system achieves address translation. (12 marks)
- b) Explain the following terms: (6 marks)
- i.) Page Fault
 - ii.) Demand Paging
 - iii.) Working set

c) In the system mentioned in 2(a) above, when you run a graphic intensive application, you notice that the hard disk LED is continuously blinking and the system response is degraded noticeably. What do you call this state as far as the system is concerned. State the reason for this state and what do you recommend to resolve this situation? (3 marks)

d) Differentiate between the page replacement algorithms FIFO and LRU? (4 marks)

Total 25 marks

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3.

- a) Draw a schematic diagram to show the motherboard architecture of a typical modern PC, showing multi-bus system, Chipset (North & South bridges), memory, CPU, and devices.

Explain briefly about each component. (20 marks)

- b) List the standard hardware interrupts and I/O Ports allocation in a PC (5 marks)

Total 25 marks

4.

- a) What is multitasking in RTOS? (3 marks)

- b) Explain the following terms: (8 marks)

- i.) Co-operative Multitasking
- ii.) Pre-emptive Multitasking

- c) How does the semaphore work? (6 marks)

- d) What is a scheduler? Draw the state diagram showing the relationship between the tasks in a pre-emptive scheduler. (8 marks)

Total 25 marks

5.

- a) Explain the Following input/output techniques and give advantages and disadvantages of each. (15 marks)

- i) Polling
- ii) Interrupt
- iii) DMA

- b) Describe Handshaking with help of a timing diagram how synchronous data transfer takes place between a computer system and its peripherals. (10 marks)

Total 25 marks

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6.

- a) What is instruction *pipelining*? What are the six stages of instruction processing? Explain each stage with the help of diagram showing the logical sequence and unconditional branching. (8 marks)
- b) Draw the state-space diagram of a six-stage pipeline, processing nine instructions with no branching. Show the number cycles saved using pipelining. (8 marks)
- c) Explain the effect of a conditional branch instruction in the above state-space diagram. (4 marks)
- d) Determine the speed up factor for a six-segment pipeline with a clock cycle of 10 ns for each stage, processing 200 tasks with no branches. Assume the corresponding non-pipeline system takes 60 ns to process a task. (5 marks)

Total 25 marks

END OF QUESTIONS