

UNIVERSITY OF BOLTON (RAK)

**SCHOOL OF THE BUILT ENVIRONMENT &
ENGINEERING – RAK CAMPUS**

**BENG(HONS) ELECTRONIC & COMPUTER
ENGINEERING**

SEMESTER 3 EXAMINATION 2010-2011

COMPUTER ENGINEERING

MODULE NO: ECE3046

Date: Tuesday, 30 August 2011

Time: 13.00 – 15.00

INSTRUCTIONS TO CANDIDATES:

There are SIX questions on this paper

Answer ANY FOUR questions.

All questions carry equal marks.

Marks for parts of questions are shown in brackets.

Unless otherwise stated all symbols take their usual meaning.

Electronic calculators may be used provided that data and program storage memory is cleared prior to the examination.

1. (a) Draw a diagram showing the hierarchy of memory and other storage devices within a typical computer system.

(3 marks)

- (b) List the major characteristics of dynamic RAM and static RAM and indicate where, in a modern PC memory system, these two types of RAM are used. Illustrate your answer with diagrams of the cell structure of each.

(12 marks)

- (c) A small computer has the following memory and I/O components interfaced to the CPU via the bus systems:-

32 Kbytes of ROM starting at address 8000h

16 Kbytes of RAM implemented by 2 X 8 Kbyte chips in contiguous memory locations starting at address 0000h

32 bytes of memory-mapped I/O starting at address 5000h

Draw the system memory map and design a decoder circuit to generate the necessary chip-select signals (active low).

(10 marks)

Total 25 Marks

Please turn the page

2. (a) A 32-bit system uses a 2048 entry direct mapped L2 cache with each line holding 32 bytes of data. Design the required virtual address format showing the number of bits in each field and their position in the physical address.

(6 marks)

- (b) During part of a program run on the machine described in Q2(a) the following 32-bit physical addresses in main memory are accessed and their data copied to cache:-

26F41E2A, 612E5B17, 0B1F2CE5

If the following addresses are subsequently accessed determine which can retrieve data from the cache:-

612E5B0A, 26F41E39, 0B1F26D4, 26F41E3A, 612E5B20

(14 marks)

- (c) A system's main memory, M, has an access time of 90nS and a cache memory, C, has an access time of 10nS with a hit ratio, H, of 85%. Derive an expression for the average access time, A, and calculate that value.

(5 marks)

Total 25 marks

Please turn the page

3. (a) List the six steps involved in the processing of a typical instruction and draw a space - time diagram for a six-segment pipeline showing the time it takes to process nine tasks. Compare this time taken with pipelining against that without pipelining. (7 marks)
- (b) Using a similar space – time diagram to that used in Q3(a) explain the effect of a conditional branch instruction on the pipeline operation. (7 marks)
- (c) A non-pipeline system takes 60 ns to process a task. The same task can be processed in a six – segments pipeline with a clock cycle of 8 ns. Assuming that no branches are taken, determine the speed up factor of the pipeline for 200 tasks. What is the maximum speedup that can be achieved? (6 marks)
- (d) Draw a state diagram that represents an algorithm for branch prediction using two history bits. (5 marks)

Total 25 marks

4. (a) Describe, using a diagram, how the basic mechanism of the stack is used during nested subroutine calls and interrupts. (8 marks)
- (b) Explain how a stack is used as a dynamic data store for local variables during procedures. (7 marks)
- (c) A stack is often used for expression evaluation in a CPU using postfix (reverse-Polish) notation. State the 2 rules which must be applied to evaluate a postfix notation expression. Convert the expression, $(A-B)/(C-D)$ to postfix notation and show how the resulting expression is evaluated using a stack. (10 marks)

Total 25 marks

Please turn the page

5. (a) Describe the 3 input/output techniques listed below giving advantages and disadvantages of each:-
- i) Polling (5 marks)
 - ii) Interrupt (5 marks)
 - iii) Direct Memory Access (DMA) (5 marks)
- (b) Using a timing diagram to illustrate your answer describe the method of handshaking to synchronise data transfers between a computer system and its peripherals. (10 marks)

Total 25 marks

6. (a) Describe the operation of the circuit of Fig.Q6 by showing the contents of each register during each clock cycle of the calculation with a multiplicand of 1001 and a multiplier of 1011. (10 marks)

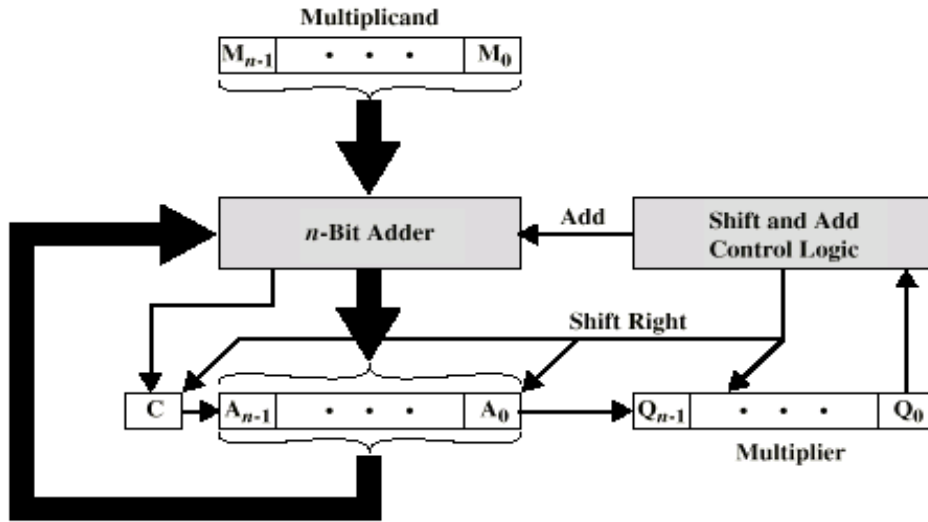


Fig. Q6 Shift and Add Multiplier

- (b) State the rules for multiplication of 2's complement numbers using Booth's algorithm. (8 marks)
- (b) Use Booth's algorithm to evaluate (-4×-5) in 2's complement arithmetic. Show all working. (7 marks)

Total 25 marks

END OF QUESTIONS